AMENDMENTS TO THE SPECIFICATION:

Please amend the 13th paragraph on page 5 as follows:

In Fig. 1, which illustrates a prior art output buffer apparatus (see: JP-A-2002-94366), a pre-buffer circuit receives a data signal D from an internal circuit (not shown), pull-up impedance adjusting signals RUP1, RUP2, ..., RUPn and pull-down impedance adjusting signals RDN1, RDN2, ..., RDNn to generate pull-up signals P1, P2, ..., Pn and pull-down signals D1, D2, ..., Dn. The pull-up signals P1, P2, ..., Pn and the pull-down signals D1, D2, ...Dn are supplied to a main-buffer circuit 2 which, in turn, generates an output signal ~~signals~~ at the output terminal OUT.

Please amend the 2nd paragraph on page 6 as follows:

As illustrated in Fig. 2, which is a detailed circuit diagram of the pre-buffer circuit 1 (the dummy pre-buffer circuit 32) of Fig. 1, the pre-buffer circuit 1 (the dummy pre-buffer circuit 32) is constructed by n-stage pre-drivers 11, 12, ..., 1n each receiving the data signal D (the dummy data signal D′), one of the pull-up impedance adjusting signals RUP1, RUP2, ..., RUPn (RUP1', RUP2', ..., RUPn') ~~PUP1, PUP2, ..., PUPn (PUP1′, PUP2′, ..., PUPn′)~~ and one of the pull-down impedance adjusting signals RDN1, RDN2, ..., RDNn (RDN1', RDN2', ... RDNn') ~~PDN1, PDN2, ..., PDNn (PDN1′, PDN2′, ..., PDNn′)~~. In more detail, the pre-driver 1i (i = 1, 2, ..., n) is constructed by two transfer gates 101 and 102 connected in series powered by the data signal D (the dummy data signal D′) and a high power supply voltage V_{DD}, and two inverters 103 and 104 for receiving the pull-up impedance adjusting signals RUPi (RUPi′) to turn ON one of the transfer gates 101 and 102 and turn OFF the other. Also, the pre-driver 1i (i = 1, 2, ..., n) is constructed by two transfer gates 105 and 106 connected in series powered by the data signal D (the dummy data signal D′) and a ground voltage GND, and two inverters 107 and 108 for

receiving the pull-down impedance adjusting signals RDNi to turn ON one of the transfer gates 105 and 106 and turn OFF the other.

Please amend the first paragraph on page 7 as follows:

For example, as illustrated in Fig. 3A, when the pull-up impedance adjusting signal RUPI (RUPi') ~~PUPi (PUPi')~~ is "1" (high) and the data signal D (D') is "0" (low), the transfer gates 101 and 102 are turned ON and OFF, respectively, so that the pull-up signal Pi (Pi') is low (activating level). On the other hand, when the pull-up impedance adjusting signal RUPI (RUPi') ~~PUPi (PUPi')~~ is "1" (high) and the data signal D (D') is "1" (high), the transfer gates 101 and 102 are turned OFF and ON, respectively, so that the pull-up signal Pi (Pi') is high (deactivating level). Note that, if the data signal D (D') is high, the pull-up signal Pi (Pi') is high (deactivating level) regardless of the pull-up impedance adjusting signal RUPI (RUPi') ~~PUPi (PUPi')~~.

Please amend the first paragraph on page 8 as follows:

Similarly, as illustrating in Fig. 3B, when the pull-down impedance adjusting signal RDNi (RDNi') ~~PDNi (PDNi')~~ is "1" (high) and the data signal D (D') is (high), the transfer gates 105 and 106 are turned ON and OFF, respectively, so that the pull-down signal Ni (Ni') is high (activating level). On the other hand, when the pull-up impedance adjusting signal RUPI (RUPi') ~~PUPi (PUPi')~~ is "1" (high) and the data signal D (D') is low, the transfer gates 105 and 106 are turned OFF and ON, respectively, so that the pull-down signal Ni (Ni') is low (deactivating level). Note that, if the data signal D (D') is low ~~high~~ the pull-down signal Ni (Ni') is low (deactivating level) regardless of the pull-down impedance adjusting signal RDNi (RDNi') ~~PDNi (PDNi')~~.

Please amend the fourth paragraph on page 8 as follows:

For example, as illustrated in Fig. 5, when the pull-up signal Pi (Pi′) is low (activating level) and the pull-down signal Ni is low (deactivating level), the transistors 201 and 202 are turned ON and OFF, respectively, so that the voltage at the output terminal OUT is high. On the other hand, when the pull-up signal Pi (Pi′) is high (deactivating level) and the pull-down signal Ni is high (activating level), the transistors 201 and 202 are turned OFF and ON, respectively, so that the voltage at the output terminal OUT is low. Note that the pull-up signal Pi (Pi′) and the pull-down signal Ni (Ni′) are never at the activating levels simultaneously, i.e., which is forbidden. Also, when the pull-up signal Pi (Pi′) is high (deactivating level) and the pull-down Ni (Ni′) is low (deactivating ~~activating~~ level), the output terminal OUT is in a high impedance (HZ) state.

Please amend the fourth paragraph on page 11 as follows:

The D-type flip-flop 1i-1 (i = 1, 2, ..., n) has a data input D for receiving the pull-up impedance adjusting signal RUPi, a clock terminal C for receiving the data signal D and an output terminal Q for generating an output signal which is transmitted to the inverter 103 of the pre-driver 1i. That is, the pull-up impedance adjusting signal RUPi ~~PUPi~~ is fetched by the D-type flip-flop 1i-1 in synchronization with a falling edge of the data signal D.

Please amend the fourth paragraph on page 13 as follows:

The operation of the latch circuit 1i′-1(i = 1, 2, ..., n) is explained next with reference to Fig. 14B. That is, when the data signal D is "0" (low), the transfer gates 1404 and 1407 are turned OFF and ON, respectively, so that the latch circuit 1i′-1 is in a hold state. Therefore, the signal at the output terminal Q is the same as the pull-up impedance adjusting signal RUPi ~~PUPi~~ immediately before the data signal D is switched from "1" (high) to "0" (low). On the other hand, when the data signal D is "1" (high), the transfer gates 1404 and 1407 are turned ON and

OFF, respectively, so that the latch circuit 1i'-1 is in a through state. Therefore, the signal at the output terminal Q is always the same as the pull-up impedance adjusting signal RUPi ~~PUPi~~.

Please amend the second paragraph on page 14 as follows:

The operation of the latch circuit 1i'-2(i = 1, 2, ..., n) is explained next with reference to Fig. 15B. That is, when the data signal D is "0" (low), the transfer gates 1414 and 1417 are turned ON and OFF, respectively, so that the latch circuit 1i'-2 is in a through state. Therefore, the signal at the output terminal Q is always the same as the pull-down impedance adjusting signal RDNi ~~PDNi~~. On the other hand, when the data signal D is "1" (high), the transfer gates 1414 and 1417 are turned OFF and ON, respectively, so that the latch circuit 1i' - 2 ~~1i'-1~~ is in a hold state. Therefore, the signal at the output terminal Q is the same as the pull-down impedance adjusting signal RDNi ~~PDNi~~ immediately before the data signal D is switched from "0" ~~"1"~~ (low) to "1" (high) ~~"0" (low)~~.

Please fourth the first paragraph on page 15 as follows:

That is, the impedance code RUP is fetched at periods t2 to t3, t4 to t5, t6 to t7, t8 to t8', t10 to t11, t12 to t13, t14 to t15, t16 to t17 when the data signal D is "0" (low). On the other hand, the impedance code RDN ~~RDP~~ is fetched at periods t1 to t2, t3 to t4, t5 to t6, t7 to t8, t9 to t10, t11 to t12, t13 to t14, t15 to t16 when the data signal D is "1" (high).

Please fourth the second paragraph on page 15 as follows:

In the calibrating operation as illustrated in Fig. 16, when the impedance code RUP ~~RUN~~ is changed as indicated by Y1, Y2, ... in Fig. 16 while the data signal D continues at the value "0" (low), the changed code RUP ~~RUN~~ is fetched, and also, when the impedance code RDP is changed as indicated by Z1, Z2, ... in Fig. 16 while the data signal D continues at the value "1"

(high), the changed code RDP is fetched. Therefore, a discrepancy between the output impedance of the output buffer apparatus and the characteristic impedance of the transmission line may be suppressed which would suppress reflection noise at the terminal of the transmission line.